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10/657,510	09/05/2003	William C. Moyer	SC13053TH	9320

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EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	PAPER NUMBER
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/657,510	MOYER, WILLIAM C.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/23/07 and 12/05/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed February 6th 2007. Claims 1-44 are pending. Applicant's arguments have been carefully and respectfully considered, but they are not entirely persuasive, as will be discussed in more detail below. Accordingly, this action has been made FINAL.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by **M.P.E.P.** 609(c), the examiner acknowledges the applicant's submission of the Information Disclosure Statements dated **03/23/2007 and 12/05/2006** have been considered in the examination of the claims now pending. As required by **M.P.E.P.** 609(c), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14, 17-18, 21-23, and 30-35, 37-38, and 40-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida et al. (U.S. Patent no. 5,475,852, hereafter referred to as Yoshida).

Independent Claims

With respect to **independent claims 1 (30 and 41),**

> *"A data processing system comprising: a memory for storing operands;* **[disclosed e.g. in column 8, lines 17-25]** *at least one general purpose register;* **[disclosed in column 11, lines 37-39, "FIG. 12 is a schematic diagram of the format thereof. Each symbol Rn 272a, 272b shows the number of the general-purpose register."]** *and processor circuitry for executing one or more instructions,* **[disclosed in column 9, lines 23-24, "FIG. 3 is a schematic diagram showing a format 208 of an operational instruction between memory and register."]** *at* least one of the one or more instructions **[i.e. "E-format" and "I-format" disclosed in column 10, lines 26-43]** *for transferring data elements between the memory and the at least one general purpose register* **[disclosed in column 9, lines 23-24, "FIG. 3 is a schematic diagram showing a format 208 of an operational instruction between memory and register."]** *wherein the at least one or more instructions specifies size of data elements in the memory separate and independent from specifying size of data elements in the at least one general purpose register."* **[disclosed, e.g. in column 9, lines 28-36, and column 11, lines 40-50.]**

Dependent Claims

With respect to **claims 2 (31 and 42)**,

"The data processing system of claim 1 wherein the one or more instructions comprises independent fields for separately storing a first data size specifier for the memory and a second data size specifier for the at least one general purpose register." **[disclosed, e.g. in column 9, lines 28-36, "In the L-format, symbol Sh 210 represents the designating field of the source operand, symbol Rn 212 represents the designating field of the register of the destination operand and RR 214 represents designating of the operand size of Sh 210, respectively. The size of the destination operand located in the register is fixed to 32 bits. Where the size of the register side differs from that of the memory side and the size of the source side is smaller, sign extension is performed."]**

With respect to **claims 3 (32 and 42)**,

"The data processing system of claim 1 wherein the one or more instructions specifies a storage location for defining a first data size specifier for the memory and a second data size specifier for the at least one general purpose register." **[disclosed, e.g. in column 9, lines 28-36, "In the L-format, symbol Sh 210 represents the designating field of the source operand, symbol Rn 212 represents the designating field of the register of the destination operand and RR 214 represents designating of the operand size of Sh 210, respectively." The designating fields of the source and destination are**

interpreted as storage locations for the first and second data specifiers as claimed.]

With respect to **claim 4,**

"The data processing system of claim 3 wherein the storage location is any one of a location in the memory and a processor register location external to the memory." **[disclosed, e.g. in column 2, lines 2-4, "the operand access unit 104 outputs the operand address to the memory external to the microprocessor..."]**

With respect to **claim 5**,

"The data processing system of claim 3 wherein the storage location is a control register of the data processing system." **["FIG. 4 is a schematic diagram showing a format 216 of an operational instruction between register and register (R-format)." Yoshida shows a storage location is a register]**

With respect to **claim 6**,

"The data processing system of claim 3 wherein the storage location is a register within the data processing system that arithmetic, logical and shift operations performed by the data processing system utilize." **[disclosed, e.g. in column 17, lines 43-47]**

With respect to **claim 7**,

"The data processing system of claim 1 wherein the memory further comprises a plurality of multiple data elements to be transferred between the memory and the at least one general purpose register." **[Yoshida teaches this claim, e.g. in FIG. 50, step s51]**

With respect to **claims 8 (and 33)**,

"The data processing system of claim 7 wherein the multiple data elements are contiguous in the memory." **[see column 14, lines 27-30]**

With respect to **claims 9 (and 34)**,

"The data processing system of claim 7 wherein the multiple data elements are non-contiguous in the memory." **[FIG. 27 shows data elements "IRL" and "Micro Rom Address" as *non-contiguous* in memory]**

With respect to **claim 10**,

"The data processing system of claim 1 wherein each of the at least one general purpose register holds multiple data elements." **[Yoshida teaches this claim, e.g. in FIG. 50, step s51. Also see column 16, lines 65-67]**

With respect to **claim 11**,

"The data processing system of claim 1 wherein each of the at least one general purpose register comprises a scalar register that has a one-dimensional memory map." **[FIG. 2 shows a *scalar register* that has a one-dimensional, single row bit field.]**

With respect to **claim 12**,

"The data processor of claim 1 wherein when the at least one or more instructions specifies size of a source data element in the memory to be greater than size of a destination data element in the at least one general purpose register, the processor circuitry truncates a portion of the source data element in the memory." **[disclosed in column 9, lines 42-45, "Where the size of the register side differs from that of the memory side and the size of the source side is larger, truncating of the overflow portion and overflow check are performed."]**

With respect to **claim 13**,

"The data processor of claim 12 wherein the portion of the source data element in the memory that is truncated is a high order portion of the source data element in the memory." **[disclosed in column 9, lines 42-45, "Where the size of the register side differs from that of the memory side and the size of the source side is larger, truncating of the overflow portion and overflow check are performed." The high order portion of the source data element is interpreted as either the overflow portion as disclosed in Yoshida.]**

With respect to **claim 14**,

"The data processor of claim 12 wherein the portion of the source data element in the memory that is truncated is a low order portion of the source data element in the memory." **[disclosed in column 9, lines 42-45, "Where the size of the**

register side differs from that of the memory side and the size of the source side is larger, truncating of the overflow portion and overflow check are performed." The low order portion of the source data element is interpreted as either the overflow check as disclosed in Yoshida.]

With respect to **claim 17**,

"The data processor of claim 16 wherein the processor circuitry places predetermined data values in the portion of the destination data element of the at least one general purpose register by using zero extension." **[Yoshida anticipates this limitation e.g. in column 9, lines 59-67]**

With respect to **claim 18**,

"The data processor of claim 16 wherein the processor circuitry places predetermined data values in the portion of the destination data element of the at least one general purpose register by using sign extension." **[Yoshida discloses, e.g. in column 9, lines 32-36]**

With respect to **claim 21**,

"The data processor of claim 1 wherein when the at least one or more instructions specifies size of a destination data element in the memory to be less than a size of a source data element in the at least one general purpose register, the processor circuitry truncates a portion of the source data element in the at least one general purpose register." **[disclosed in column 9, lines 42-45, "Where the size of the register side differs from that of the memory side**

and the size of the source side is larger, truncating of the overflow portion and overflow check are performed." Yoshida teaches that the general purpose register is a source.]

With respect to **claim 22**,

"The data processor of claim 21 wherein the processor circuitry truncates a high order portion of the source data element in the at least one general purpose register." **[disclosed in column 9, lines 42-45, "Where the size of the register side differs from that of the memory side and the size of the source side is larger, truncating of the overflow portion and overflow check are performed." The high order portion of the source data element is interpreted as either the overflow portion as disclosed in Yoshida.]**

With respect to **claim 23**,

"The data processor of claim 21 wherein the processor circuitry truncates a low order portion of the source data element in the at least one general purpose register." **[disclosed in column 9, lines 42-45, "Where the size of the register side differs from that of the memory side and the size of the source side is larger, truncating of the overflow portion and overflow check are performed." The low order portion of the source data element is interpreted as either the overflow check as disclosed in Yoshida.]**

With respect to **claim 44**,

> *"The data processing system of claim 41 further comprising control circuitry that adjusts data element size when necessary to communicate data when size of data elements stored in the memory differ from size of data elements stored in the at least one storage location in the data processing system external to the memory."* **[Yoshida teaches the above claim, e.g. in column 1, lines 62-67]**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 16, 19, 20, and 25-29 are rejected under 35 U.S.C. 103(a) as being obvious over Yoshida et al. (U.S. Patent no. 5,475,852 in view of the Chung et al. (U.S. Patent No. 6,950,922, hereafter referred to as Chung).

With respect to **claims 16, 19, 20, and 25, 28-29,** Yoshida teaches "The data processor of claim 1" as stated supra in the rejection to claim 1.

Yoshida, however, does not disclose *expressly* the limitations of claims **16, 19, 20, and 25, 28-29, which are taught by Chung as shown below.**

Yoshida and Chung are *analogous art* because they are from the same field of endeavor, that being source to destination register memory copying.

At the time of the invention it would have been *obvious* to a person of ordinary skill in the art to combine the functions of claims 16, 19, and 20 with claim 1.

The *motivation* for doing so would have been obvious based on the teaching of Chung in column 1, lines 38-52.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Yoshida and Chung before him/her to combine Chung and Yoshida for the benefit of having the claim limitations found in claims 16, 19, and 20 (which also encompass the limitations of claims 25-29) which depend upon claim 1.

With respect to **claim 16**,

> *"The data processor of claim 1 wherein when the at least one or more instructions specifies size of a source data element in the memory to have a*

smaller size than a destination data element in the at least one general purpose register, the processor circuitry places predetermined data values in a portion of the destination data element of the at least one general purpose register that is not filled by the source data element from the memory." **[disclosed in Chung in column 9, lines 47-53]**

With respect to **claim 19**,

"The data processor of claim 16 wherein the processor circuitry places predetermined data values in the portion of the destination data element of the at least one general purpose register by filling a predetermined bit value in a low order data portion of the destination data element of the at least one general purpose register." **[See Chung FIG. 2, element 220 and all associated text within the specification]**

With respect to **claim 20**,

"The data processor of claim 19 wherein the predetermined bit value is a zero value." **[Disclosed in Chung column 9, lines 1-25]**

With respect to **claim 25**,

"The data processor of claim 1 wherein when the at least one or more instructions specifies size of a destination data element in the memory to be greater than a size of a source data element in the at least one general purpose register, the processor circuitry places predetermined data values in a portion of the destination data element in the memory that is not filled by the source data

element in the at least one general purpose register." **[disclosed in Chung in column 9, lines 47-53]**

With respect to **claim 26**,

"The data processor of claim 25 wherein the processor circuitry places the predetermined data values in the portion of the destination data element in the memory that is not filled by using zero extension." **[Yoshida anticipates this limitation e.g. in column 9, lines 59-67]**

With respect to **claim 27**,

"The data processor of claim 25 wherein the processor circuitry places the predetermined data values in the portion of the destination data element in the memory that is not filled by using sign extension." **[Yoshida discloses, e.g. in column 9, lines 32-36]**

With respect to **claim 28**,

"The data processor of claim 25 wherein the processor circuitry places the predetermined data values in the portion of the destination data element in the memory that is not filled by placing a predetermined bit value in a low order data portion of the destination data element." **[See Chung FIG. 2, element 220 and all associated text within the specification]**

With respect to **claim 29**,

"The data processor of claim 28 wherein the predetermined bit value is zero."

[Disclosed in Chung column 9, lines 1-25]

Claims 15, 24, 36, and 39 are rejected under 35 U.S.C. 103(a) as being obvious over Yoshida et al. (U.S. Patent no. 5,475,852 in view of Paver et al. (U.S. Patent No. 6,950,922, hereafter referred to as Paver).

With respect to **claims 15, 24, 36, and 39,** Yoshida teaches "The data processor of claim 1" as stated supra in the rejection to claim 1.

Yoshida, however, does not disclose *expressly* the limitations of "*...the processor circuitry rounds a high order portion of the source data element in the memory based on a value of a low order portion of the source data element in the memory", as* stated in claims 15 and 24.

Paver teaches the above limitations as shown below.

Yoshida and Paver are *analogous art* because they are from the same field of endeavor, that being source to destination register memory copying.

At the time of the invention it would have been *obvious* to a person of ordinary skill in the art to combine the functions of *rounding of a portion of a source data element when determining the source to destination data specification size with the limitations of claim 1.*

The *motivation* for doing so would have been obvious based on the teaching of Paver in column 1, lines 15-34.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of Yoshida and Paver before him/her to combine Paver and Yoshida for the benefit of having a limitation *rounding of a portion of a source data element when determining the source to destination data specification size with the limitations of claim 1.*

With respect to **claims 15 (and 36)**,

> *"The data processor of claim 1 wherein when the at least one or more instructions specifies size of a source data element in the memory to be greater than the size of a destination data element in the at least one general purpose register, the processor circuitry rounds a high order portion of the source data element in the memory based on a value of a low order portion of the source data element in the memory."* **[disclosed by Paver in column 8, lines 24-36]**

With respect to **claims 24 (and 39)**,

> *"The data processor of claim 1 wherein when the at least one or more instructions specifies size of a destination data element in the memory to be less than a size of a source data element in the at least one general purpose register, the processor circuitry rounds a high order portion of the source data element in the at least one general purpose register based on a value of a low order portion of the source data element."* **[disclosed by Paver in column 8, lines 24-36]**

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

1ST POINT OF ARGUMENT:

With respect to the arguments on page 2 of the applicant's remarks, the examiner respectfully disagrees that Yoshida fails to disclose specifying a size of data elements in a general purpose register as recited in claim 1. Yoshida teaches in column 11, lines 40-50 displacement values of the general purpose register which specify the size (either 16 or 32 bits) of the data elements. Although Yoshida teaches that the size of the *destination* operand located in the register is fixed, this teaching only applies to a singular type of instruction format type ("L-format" disclosed in column 9, lines 23-27). Yoshida also teaches information format types ("E-format" disclosed in column 10, lines 26-43) in which the sizes of the data elements are specified separately in both the memory and the general purpose registers. Yoshida discloses in column 10, lines 33-43, "...E-format presupposes an operation between different seizes, and the source operand of eight bits is zero-extended or sign-extended in a manner of agreeing with the size of the destination operand." Consequently, Yoshida's teachings anticipate the claim language of the independent claims.

2nd POINT OF ARGUMENT:

With respect to the arguments on page 3 in regard to claims 2-14, 17-18, and 21-23, see the clarified arguments above for claim 1. Arguments found on page 3 of the applicant's remarks stand rejected under the same arguments.

3rd POINT OF ARGUMENT:

With respect to the arguments on pages 3-4 in regard to the obviousness rejections to claims 16, 19, 20 and 25-29, as well as claims 15, 24, 36, and 39, see the clarified arguments above for claim 1. Arguments found on pages 3 and 4 of the applicant's remarks stand rejected under the same arguments.

CONCLUSION

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

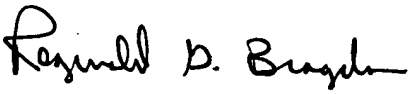
Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Reginald G. Bragdon



HLF
April 16th, 2007

Supervisory Patent Examiner
Technology Center 2100